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Press Release

Plurality's 64-Core Accelerator Delivers Market's Highest Performance per Cost, Power and Size

Tightly-coupled manycore design plus patented scheduler make HyperCore IP the ideal SoC solution for mass-market parallel applications

Grenoble, December 3, 2008 - Plurality Ltd. today announced the industry's first complete silicon Intellectual Property (IP) solution for its HyperCore™ processor, the market's most powerful, space-saving and energy-efficient 64-core shared-memory processing engine. Plurality, a developer of advanced manycore processor solutions, has made the HyperCore processor IP available to help developers rapidly integrate the general-purpose accelerator into system-on-chip (SoC) designs. The 32 GIPS, 8 GFLOPS 64-core processor acts as a performance extension to the industry's most popular processor architectures (x86, PowerPC, and ARM). The IP version of the HyperCore processor, announced here at the IP '08 IP-Based System Design Conference and Exhibition, represents a game-changing shift in the way VLSI architectures can be designed.

"HyperCore delivers performance that is tens-of-times better, and at the lowest price per watt per square millimeter, than any other chip-level, shared-memory machine currently on the market," said Plurality chairman and CEO Igor Pe'er. "With our IP, developers of SoCs, ASICs and general-purpose processors will save huge amounts of time and money in bringing the incredible power of manycore processing to mass-market applications like graphics, image and video processing, video surveillance, gaming, network processing, security, and software-defined radio."

"A pioneer in the manycore world"

The HyperCore architecture includes a patent-pending, shared-memory design in which the tightly-coupled cores are equidistant from a many-ported L1 shared-memory. Each core can randomly and directly access this memory at every clock cycle without a bottleneck. The result is a highly efficient system that is ideal for extremely fine-grained computation.

"Plurality clearly is a pioneer in the manycore world. They are helping to advance the adoption of manycore architecture by offering IP and future chips that will support a broad range of applications in an open development environment," stated Markus Levy, president of The Multicore Association™. "Their technology, combined with their activity on the Multicore Association's Executive Board, should make it much easier for semiconductor manufacturers to introduce their next-generation of massively-parallel chips," he added.

Plurality's 64-core design delivers up to 32 GIPS and 8 GFLOPS performance when operating at 500MHz in 65 nm GP process. Using high-speed libraries, an IP block with 64 cores, 16 shared floating point and multiply-accumulate units, and without memory occupies less than 12mm^2 (0.19 mm^2/core). Power consumption per-core is a mere 10 milliwatts. A 64-core design with 16 floating point units, 1 MB shared data cache and 64 KB shared instruction cache consumes about three watts and occupies only 25mm^2 (approximately 0.4mm^2/core, including the caches).

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Key to HyperCore's breakthrough performance is an architecture that features tightly-coupled cores designed to efficiently execute parallel applications. The cores are controlled by a patented hardware-based synchronizer/scheduler (US Patent 5202987), which offers many benefits. It removes management overhead from the cores, eliminates the need for an operating system, enables nearly-perfect dynamic load balancing among the cores, and facilitates task switching at very high rates, thus delivering almost linear speedup. The high-throughput, low-latency synchronizer/scheduler supports an intuitive, task-oriented programming model that facilitates the identification of parallel structures. The programming model is based on mapping the interdependencies among the identified tasks, each of which is sequential code. This task mapping enables HyperCore to take advantage of the inherent parallelism in any program.

Tools for low-cost, massively-parallel processing

Today's announcement follows the November introduction of a comprehensive set of development tools, including a cycle-accurate simulator and a software emulator, for fast evaluation of an application written in C code. The tools permit a gradual path from exploring parallel decomposition with the emulator to using the simulator for precise evaluation of the performance of a system with up to 256 cores. They can be downloaded from http://www.plurality.co.il/download_form.html.

Pricing and product availability

The 64-core IP package is available immediately and will be delivered according to the requirements of the customer. Plurality offers training, support and design services for the target process according to the customer's specific configuration. Plurality will offer IP packages with or without automatic caching, with or without floating point units. Plurality will release an FPGA-based 64-core evaluation board during Q2, 2009. The company's first chip – with 64 cores – will be introduced during the second half of 2009, along with an acceleration board that includes the 64-core chip.

About Plurality

Plurality develops advanced silicon Intellectual Property, chips and acceleration boards for manycore processing. Plurality's IP is based on a scalable, easily-programmable, manycore processor that is positioned as a general-purpose accelerator. The processor delivers the highest performance per watt per square millimeter at the lowest cost of any currently available chip-level, shared-memory machine. The privately-funded company is headquartered in Netanya, Israel. HyperCore is a trademark of Plurality Ltd. For further information, please email the company at info@plurality.com or visit www.plurality.com.

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